IJARST

International Journal of Advanced Research in Science and Technology

journal homepage: www.ijarst.com

ISSN 2319 – 1783 (Print)

ISSN 2320 – 1126 (Online)

High Speed Symmetric Convolutions based FIR Digital Filter Design

Kalpana* and KHK RaghuVamsi

Department of ECE, Koushik college of Engg.,Visakapatnam, Andhra Pradesh, India.

****Corresponding Author's Email: kalpana4692@gmail.com***

A R T I C L E I N F O

Article history:

Received 20 Nov. 2014

Accepted 11 Dec. 2014

Available online 20 Jan. 2015

Keywords:

multiple-input multiple-output (MIMO)

Fast FI Algorithms (FFA)

Finite Impulse Response (FIR) Filter

A B S T R A C T

The main challenging areas in VLSI are performance, cost, testing, area, reliability, delay and power. The demand for portable computing devices and communications system are increasing rapidly. These applications require low power dissipation and low area with high speed for VLSI circuits. Hence it is important aspect to optimize power, area and delay .So these constraints optimization became one of the main challenges. In this paper a Parallel FIR Digital Filter Structures for Symmetric Convolutions Based on Fast FIR Algorithm are designed with area, delay and power efficient. To optimize these structures a data flow HDL model is preferred because of consuming less resources when compare with other modeling schemes. This architecture is authorized in Verilog. Behavior simulation is done by using the ISE simulator and synthesis can be done by using the synthesis Xilinx ISE 9.2i.

Introduction:

The demand for high intensive data application and low power digital signal processing (DSP) is increasing day-by-day. FIR filter is the fundamental device used in DSP to meet those requirements. Many applications require FIR filter to operate at low, moderate and high frequencies. Some applications need the FIR filter to operate at high frequencies such as video processing, whereas some other applications request high throughput with a low-power circuit such as multiple-input multiple-output (MIMO) systems used in cellular wireless communication. Furthermore, when narrow transition-band characteristics are required, the much higher order in the FIR filter is unavoidable.

Two techniques of DSP applications like parallel and pipelining processing are used to reduce the power consumption. Pipelining transformation leads to a reduction in the critical path, which can be exploited to either increase the clock speed or sample speed or to reduce power consumption at same speed .Pipelining reduces the effective critical path by introducing pipelining latches along the data path .Parallel processing can be applied to digital FIR filters to either increase the effective throughput of the original filter or reduce the power consumption of the original filter .In parallel processing ,multiple outputs are computed in parallel in a clock period. Therefore, the effective sampling speed is increased by the level of parallelism .Traditionally, the application of parallel processing to an FIR filter involves the replication of the hardware units so that several inputs can be processed in parallel and several outputs can be processed at the same time. In other words, the circuit area increases linearly with the block size. .Both techniques can reduce the power consumption by lowering the supply voltage, where the sampling speed does not increase. In this paper, parallel processing in the digital FIR filter will be discussed. Due to its linear increase in the hardware implementation cost brought by the increase of the block size L, the parallel processing technique loses its advantage in practical implementation. the complexity of parallel FIR filter is reduced by the help of poly-phase decomposition, where first derive the small-sized parallel FIR filter structures and then the larger block-sized ones can be implemented by cascading or iterating small-sized parallel FIR filtering blocks. The complexity of parallel filter can be removed by the use of new class of algorithms termed as Fast FI Algorithms (FFA) and it reduce the number of multiplications with increasing the number of additions for implement the hardware. This approach is used for implement the L-parallel filter approximately (2L - 1) sub-filter blocks, each having the N/L length. The resulting parallel filtering structure would require (2N – N/L) multiplications instead of L×N. the fast linear convolution is utilized to develop the small-sized filtering structures, and then a long convolution is decomposed into several short convolutions.

However, in both categories of methods, when it comes to symmetric convolutions, the symmetry of coefficients has not been taken into consideration yet, which can lead to a significant saving in hardware cost.

In this paper we provide new parallel FIR filter structures based on FFA consisting of advantageous poly phase decomposition , which can reduce amount of multiplications in the sub filter section by exploiting the inherent nature of the symmetric coefficients, compared to the existing FFA fast parallel FIR filter structure.

2 Level Fast Fourier Algorithm:

Consider an N-tap FIR filter which can be expressed in the general form as

$$y(n) = \sum_{i=0}^{N-1} h(i)x(n-i) \quad where\, n = 0,1,2........\infty \qquad (1)$$

Where $\{x(n)\}$ is an infinite-length input sequence and $\{h(i)\}$ are the length-N FIR filter coefficients. Then, the traditional L- parallel FIR filter can be derived using polyphase decomposition as

$$\sum_{p=0}^{L-1} Y_p(\mathrm{z})^L z^{-p} = \sum_{q=0}^{L-1} X_q(\mathrm{z})^L z^{-q} . \sum_{r=0}^{L-1} H_r(\mathrm{z})^l z^{-r} \qquad (2)$$

Where $X_q = \sum_{k=0}^{\infty} z^k \ x \ LK \quad q,$

$$H_r = \sum_{K=0}^{(NL)1} z^k \ x \ LK \quad r$$

$$X_q = \sum_{k=0}^{\infty} z^{-k} x(LK+p) \quad for\ p,q,r = 0,1,2,........,L-1$$

From this FIR filtering equation, it shows that the traditional FIR filter will require L^2 -FIR sub filter blocks of length N/L for implementation.

A. 2×2 FFA (L=2)

According to (2), a two-parallel FIR filter can be expressed as

$$\begin{aligned} Y_0 + z^{-1}Y_1 &= (H_0 + z^{-1}H_1)(X_0 + z^{-1}X_1) \\ &= H_0X_0 + z^{-1}(H_0X_1 + H_1X_0) + z^{-2}H_1X_1 \end{aligned} \qquad (3)$$

Implying that

$$\begin{aligned} Y_0 &= H_0X_0 + z^{-2}H_1X_1 \\ Y_1 &= H_0X_1 + H_1X_0 \end{aligned} \qquad (4)$$

From eq (4). This structure computes a block of 2 outputs using 4 length N/2 FIR filters and 2 post processing additions, which requires 2N

multipliers and 2N − 2 adders [3].

However, (4) can be written as

$$\begin{aligned} Y_0 &= H_0X_0 + z^{-2}H_1X_1 \\ Y_1 &= (H_0 + H_1)(X_0 + X_1) - H_0X_0 - H_1X_1 \end{aligned} \qquad (5)$$

Implementation of (5) is shown in Fig. 1. This structure has three FIR sub-filter blocks of length N/2, which requires 3N/2 multipliers and 3(N/2 −1) + 4 adders. which reduces approximately one fourth over the traditional two-parallel filter hardware cost from (4). The two-parallel (L=2) FIR filter implementation using FFA obtained from (5) is shown in Fig. 1.

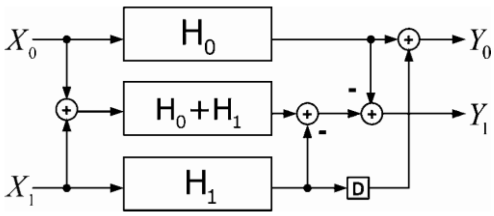


Fig. 1: Two-Parallel FIR Filter Implementation using FFA

***B. 3X3 FFA* (L=3)**

By the similar approach, a three-parallel FIR filter using FFA can be expressed as

$$\begin{aligned} Y_0 &= H_0X_0 - z^{-3}H_2X_2 + z^{-3} \\ &\quad \times\left[(H_1+H_2)(X_1+X_2) - H_1X_1\right] \\ Y_1 &= \left[(H_0+H_1)(X_0+X_1) - H_1X_1\right] \\ &\quad -\left(H_0X_0 - z^{-3}H_2X_2\right) \\ Y_2 &= \left[(H_0+H_1+H_2)(X_0+X_1+X_2)\right] \\ &\quad -\left[(H_0+H_1)(X_0+X_1) - H_1X_1\right] \\ &\quad -\left[(H_1+H_2)(X_1+X_2) - H_1X_1\right] \end{aligned} \qquad (6)$$

The hardware implementation of (6) requires six length-N/3FIR sub filter blocks, three preprocessing and seven post processing adders, and three N multipliers and 2N+4 adders, which has reduced approximately one third over the traditional three-parallel filter hardware cost. The implementation obtained from (6) is shown in Fig. 2.

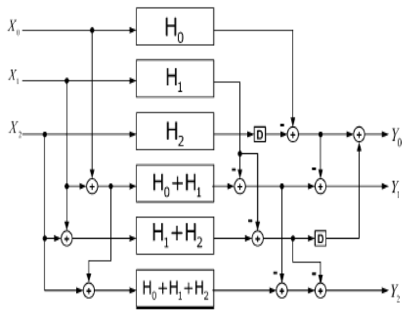


Fig: 2. Three parallel FIR filter implementation using FFA.

Symmetric of Proposed System:

A new structure is proposed to utilize the symmetry of coefficients. Poly-phase decomposition is manipulated to earn many sub filter blocks, which contain the symmetric coefficients. So half the number of multiplications can be reused in the sub-filter block for the multiplication of whole taps. Therefore, for an Ntap L-parallel FIR filter the total amount of saved multipliers is half the number of multiplications in a single sub-filter block (N/2L).

A. 2×2 Proposed FFA (L = 2)

From (4), A two-parallel FIR filter can be written as

$$Y_0 = \{\frac{1}{2}(H_0+H_1)(X_0+X_1)+ (H_0-H_1)(X_0-X_1)-H_1X_1\}+z^{-2}H_1X_1$$

$$Y_1 = \{\frac{1}{2}(H_0+H_1)(X_0+X_1)+ (H_0-H_1)(X_0-X_1)\} \quad (7)$$

When it comes to a set of even symmetric

Coefficients, (7) can can earn one more sub-filter block containing symmetric coefficients (5) than the existing

FFA parallel FIR filter. Fig. 3 shows implementation of the proposed two-parallel FIR filter based on (7).

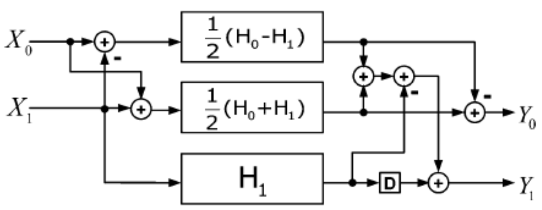


Fig. 3: Proposed Two-Parallel FIR Filter Implementation

Consider an example demonstrated here for a clearer perspective. Consider a 24-tap FIR filter with a set of sym- metric coefficients as follows:

$$\{h(0),h(1),h(2),h(3),h(4),h(5),\ldots\ldots\ldots h(23)\}$$

Where $h(0) = h(23),$

$h(1) = h(22),$

$h(2) = h(21),$

$h(3) = h(20),$

$h(4) = h(19),$

$h(5) = h(18),$

.

.

.

$h(11) = h(12)$

applying to the proposed structure, and the top two sub filter blocks with symmetric coefficients as

$$H_0 \pm H_1 = \{h(0) \pm h(1),\ h(2) \pm h(3),\ h(4) \pm h(5),\ \ldots,h(18) \pm h(19),\ h(20) \pm h(21),\ h(22) \pm h(23)$$

$$\text{where } h(0) \pm h(1) = \pm\ (h(22) \pm h(23))$$
$$h(2) \pm h(3) = \pm\ (h(20) \pm h(21))$$
$$h(4) \pm h(5) = \pm\ (h(18) \pm h(19))$$
$$h(6) \pm h(7) = \pm\ (h(16) \pm h(17)) \quad (8)$$

As can be seen from the example above, two of three subfilter blocks from the proposed two-parallel FIR filter structure, $H_0 - H_1$ and $H_0 + H_1$, are with symmetric coefficients now, as (8), which means the sub- filter block can be realized by Fig. 4, with only half the amount of mul-tipliers required. Each output of multipliers responds to two taps. Note that the transposed direct-form FIR filter is employed. Compared to the existing FFA two-parallel FIR filter structure, the proposed FFA structure leads to one more subfilter block which contains symmetric coefficients.

B. 3×3 Proposed FFA (L=3)

Same as (6), a three parallel FIR filter can be written as (9).

$$Y_0 = \frac{1}{2}\left[(H_0+H_1)(X_0+X_1)+(H_0+H_1)(X_0+X_1)\right]- H_1X_1+z^{-3}\{(H_0+H_1+H_2)(X_0+X_1+X_2)- (H_0+H_2)(X_0+X_2)-\frac{1}{2}\left[(H_0+H_1)(X_0+X_1) -(H_0-H_1)(X_0-X_1)-H_1X_1\right\}$$

$$Y_1 = \frac{1}{2}\left[(H_0+H_1)(X_0+X_1)-(H_0-H_1)(X_0-X_1)\right]+ +z^{-3}\left\{\frac{1}{2}\left[(H_0+H_2)(X_0+X_2)+(H_0-H_2)(X_0-X_2)\right]- \frac{1}{2}\left[(H_0+H_1)(X_0+X_1)+(H_0-H_1)(X_0-X_1)\right]+H_1X_1\right\}$$

$$Y_2 = \frac{1}{2}\left[(H_0+H_2)(X_0+X_2)-(H_0-H_2)(X_0-X_2)\right]+H_1X_1 \quad (9)$$

Fig. 5 shows implementation of the proposed 3-parallel FIR filter.When the number of symmetric coefficients N is the multiple of 3, the proposed 3-parallel FIR filter structure presented in (9) enables four subfilter blocks with symmetric coefficeints in total, whereas the existing FFA parallel FIR filter strucure has only two ones out of six subfilter blocks. A comparision figure is shown in fig6. Where the shadow blocks stand for the subfilter blocks which contain

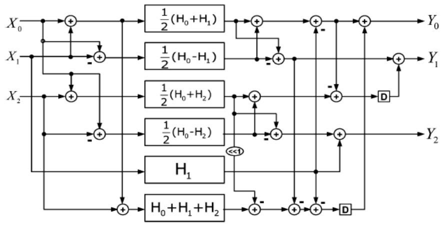


Fig. 5: Proposed three-parallel FIR filter implementation

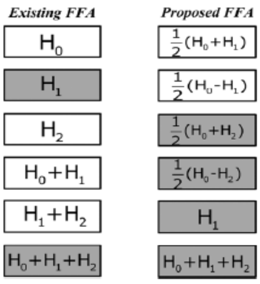


Fig.6 Comparison of sub filter blocks between existing FFA and the proposed FFA three parallel FIR structure.

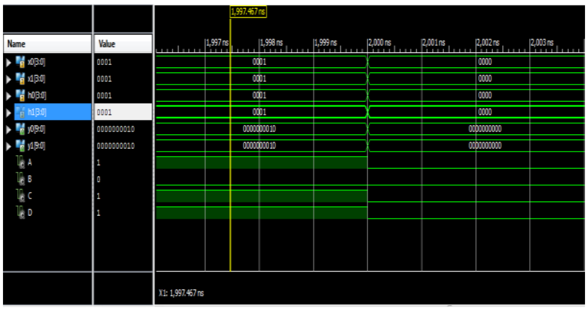
Symmetric coefficients. Therefore, for an N-tap three parallel FIR filter, the proposed structure can save N/3 multipliers from the existing FFA structure. However, again, the proposed three parallel FIR structure also brings an overhead of seven additional adders in preprocessing and post processing blocks.

C. Proposed Cascading FFA:

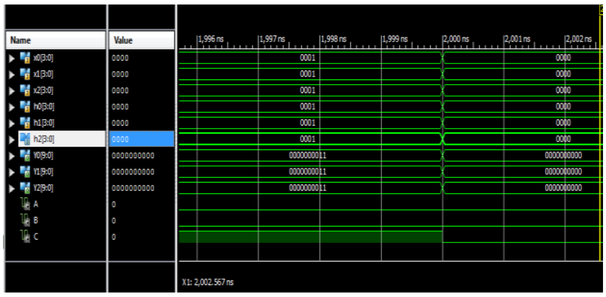
The proposed parallel FIR filter structure brings more adder cost in preprocessing and post processing blocks. It reuses the multipliers in some part of the sub-filter blocks. For larger parallel block factor L, cascading the proposed FFA parallel FIR structures increase the number of adders. So hardware complexity can be increased.

To avoid complexity, the existing FFA structures are employed for some sub-filter blocks that contain no symmetric coefficients which have more compact operations in preprocessing and post-processing blocks and the proposed FFA structures are applied to the rest of sub-filter blocks with symmetric coefficient.

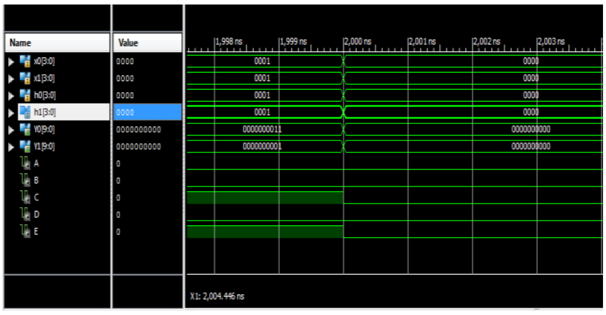
Simulation Results:



Waveform of Two Parallel FIR Filter



Waveform of Three Parallel FIR Filter



Waveform of Proposed Two- Parallel FIR Filter

Waveform of Proposed Three - Parallel FIR Filter

Conclusion:

In this paper, we have presented new parallel FIR filter structures, which are beneficial to symmetric convolutions when the number of taps is the multiple of 2 or 3. The number of increased adders stays still when the length of FIR filter becomes large, whereas the number of reduced multipliers increases along with the length of FIR filter. Finally we have reduced the area and power consumption using symmetric coefficients. In next generation using this FIR Filters we can reduce the area, power and Increasing the speed of the systems which uses FIR Filters.

About Authors:

Kalpana is a P.G student of Department of ECE, Koushik college of Engineering, Visakapatnam, Andhra Pradesh, India. And K H K Raghu Vamsi is presently working as Assistant Professor in the Department of ECE, Koushik college of Engineering, Visakapatnam, Andhra Pradesh, India.

References:

1. D. A. Parker and K. K. Parhi, "Low-area/power parallel FIR digital filter implementations," *J. VLSI Signal Process. Syst.*, vol. 17, no. 1, pp. 75–92, 1997.
2. J. G. Chung and K. K. Parhi, "Frequency-spectrum-based low-area low-power parallel FIR filter design," *EURASIP J. Appl. Signal Process.*, vol. 2002, no. 9, pp. 444–453, 2002.
3. K. K. Parhi, *VLSI Digital Signal Processing Systems: Design and Implementation*. New York: Wiley, 1999.
4. Z.-J. Mou and P. Duhamel, "Short-length FIR filters and their use in fast nonrecursive filtering," *IEEE Trans. Signal Process.*, vol. 39, no. 6, pp. 1322–1332, Jun. 1991.
5. J. I. Acha, "Computational structures for fast implementation of L-path and L-block digital filters," *IEEE Trans. Circuit Syst.*, vol. 36, no. 6, pp. 805–812, Jun. 1989.
6. C. Cheng and K. K. Parhi, "Hardware efficient fast parallel FIR filter structures based on iterated short convolution," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 51, no. 8, pp. 1492–1500, Aug. 2004.
7. C. Cheng and K. K. Parhi, "Furthur complexity reduction of parallel FIR filters," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS 2005)*, Kobe, Japan, May 2005.
8. C. Cheng and K. K. Parhi, "Low-cost parallel FIR structures with 2-stage parallelism," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol 54, no. 2, pp. 280–290, Feb. 2007.
9. I.-S. Lin and S. K. Mitra, "Overlapped block digital filtering," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process*, vol. 43, no. 8, pp. 586–596, Aug. 1996.
10. *"Design Compiler User Guide,"* ver. B-2008.09, Synopsys Inc., Sep.